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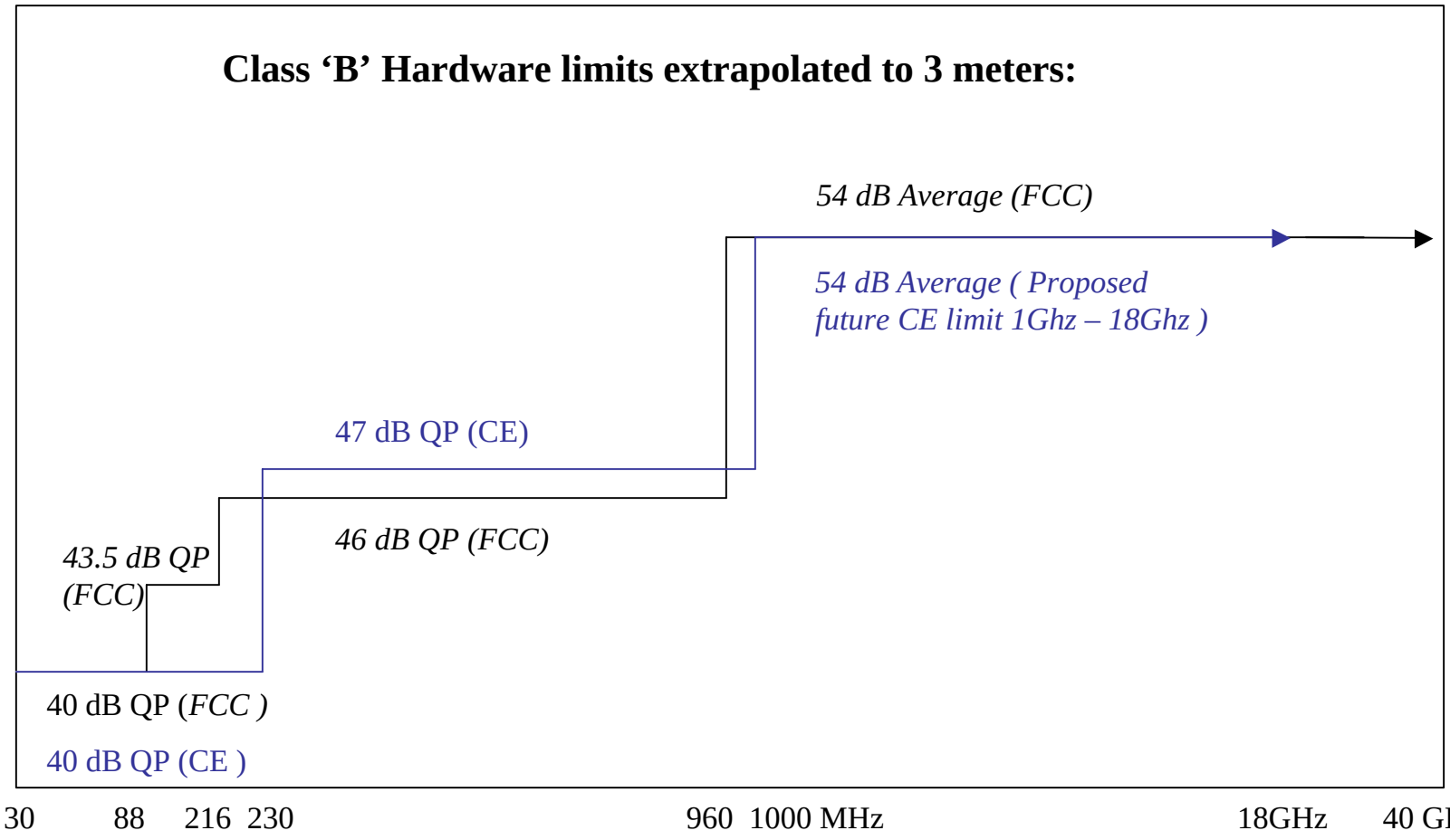
Motherboard EMC Design Essentials

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EMC… Why is it Necessary!

- All Digital Electronic Equipment must meet EMC requirements before it can be marketed for sale.
 - FCC (US & Canada)… Radiated and Conducted Requirements.
 - CE (Most of Europe)… Additional ESD / Immunity Requirements as well...
- Most challenging is meeting system Radiated Emission requirements… dBuV/m.
- Reducing Motherboard and Processor EMI levels greatly simplifies system EMC certification.

FCC/CE Radiated EMI Limits…



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EMC… Plenty of Job Security!



- Computer frequency and currents climbing.
- Marketplace pressure to limit chassis level shielding costs.
- Higher system integration places EMI source and victim closer.
- Worldwide Requirements. “No Pass” = “No Sell”

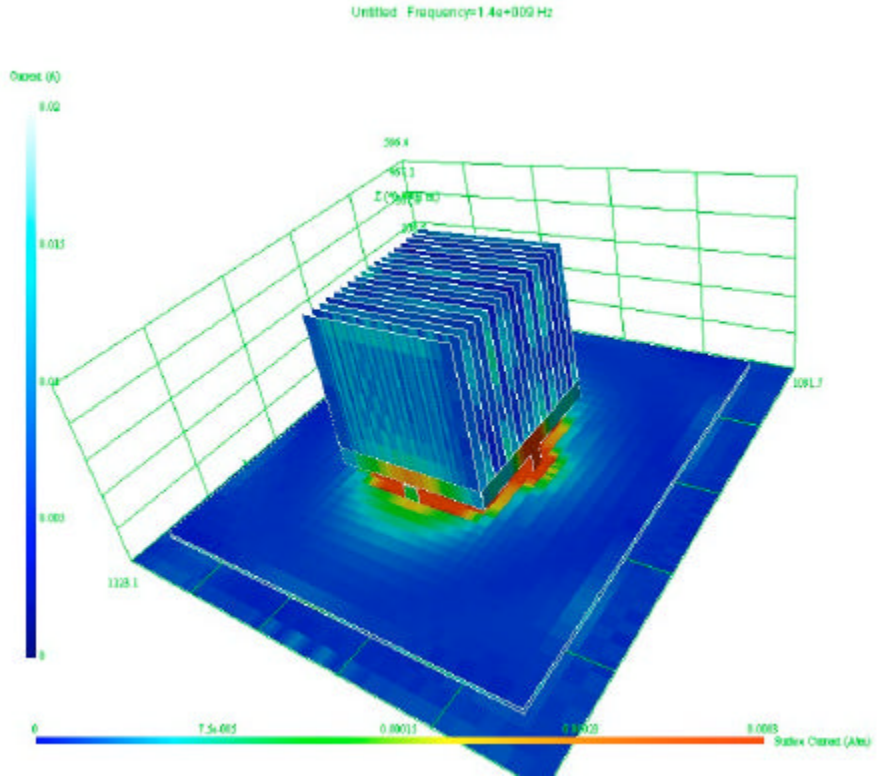
Address EMC at the Source…

- This is most efficient and economical.
- System level shielding and filtering is costly. Gaskets, cable ferrites, and extra shielding typically cost 10X or more than source level EMI suppression!
- More costly can be the lost time to market. In today's competitive market a 1 month slip can significantly reduce anticipated volume of a product.

Validating EMC Design Techniques…

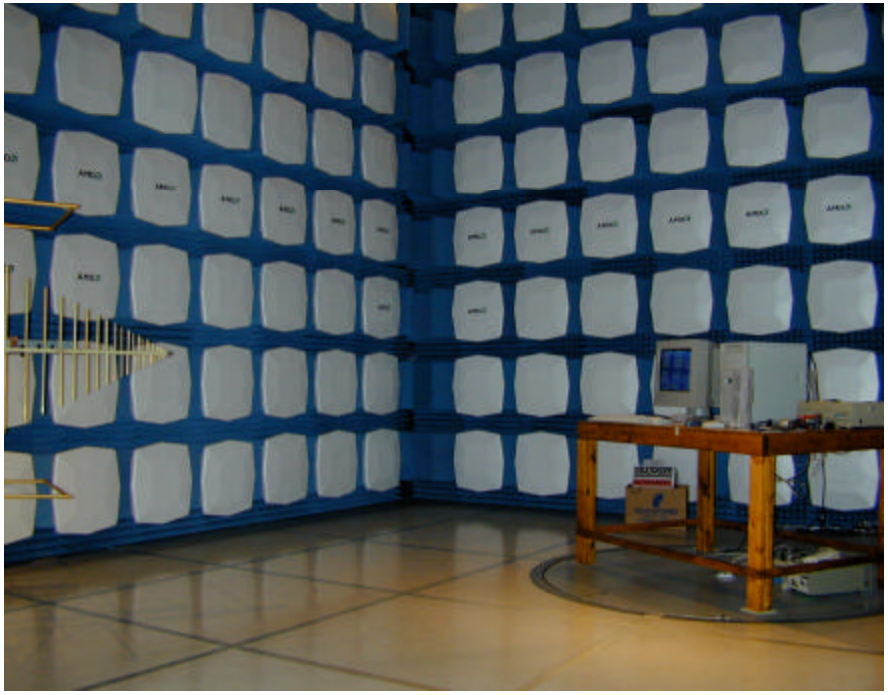
- Proven design techniques for the reduction of EMI at the PCB level.
- Validation Methods…
 - Before HW is available… Simulation tools.
 - After HW is available… EMC HW test measurements.

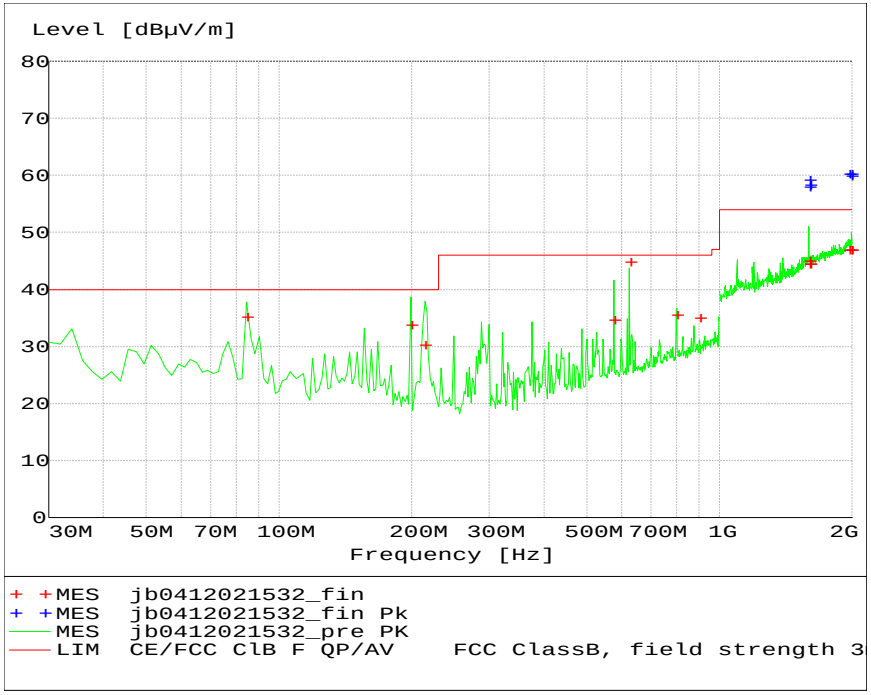
EMC Design Verification via 3D Field Simulation…



- TLM & MOM tools.
- Displays current & 3D field plots.
- Predicts potential problem areas before HW is available.

EMC Design Verification via test measurements…





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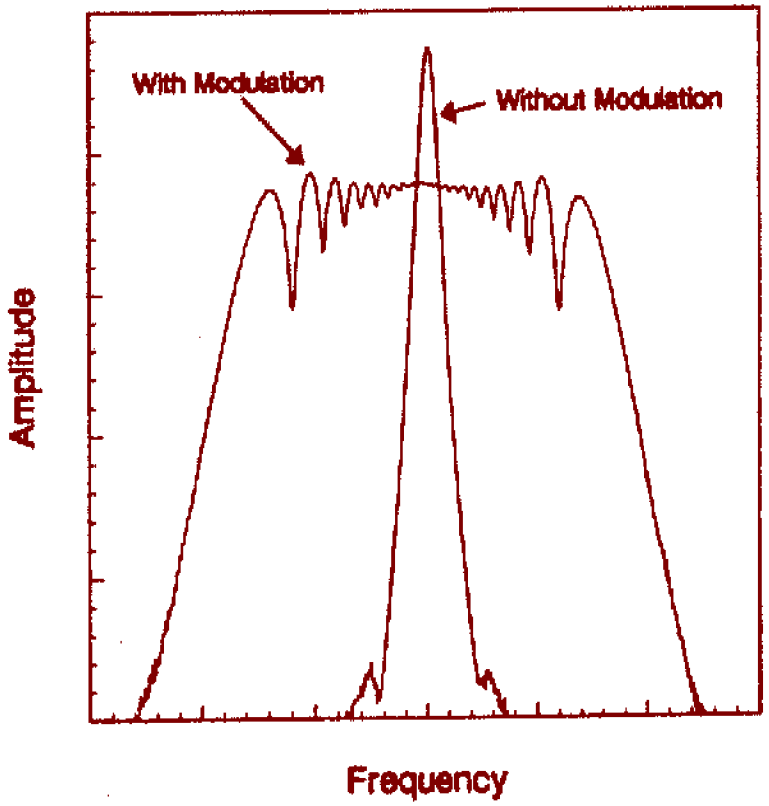
Motherboard EMC Design Techniques…



- Motherboard EMC Logic design.
- Motherboard EMC Physical design.
- CPU Specific EMC Design techniques.

Spread Spectrum Clocking…

- Controlled 30 – 50Khz clock modulation.
- Different modulating wave shapes used.
- Typically reduces system harmonics by 6dB or more!



Logic Selection and Signal Termination…

- Limit the use of high speed glue logic. Question the use of AC, ACT, or FCT logic. Often S/LS, HC/HCT, or even F can often be substituted with lower noise levels.
- Include series terminating resistors on all single ended high speed clocks. Matching the trace to clock driver impedance reduces ringing and reflections.

Keeping I/O Signals clean…

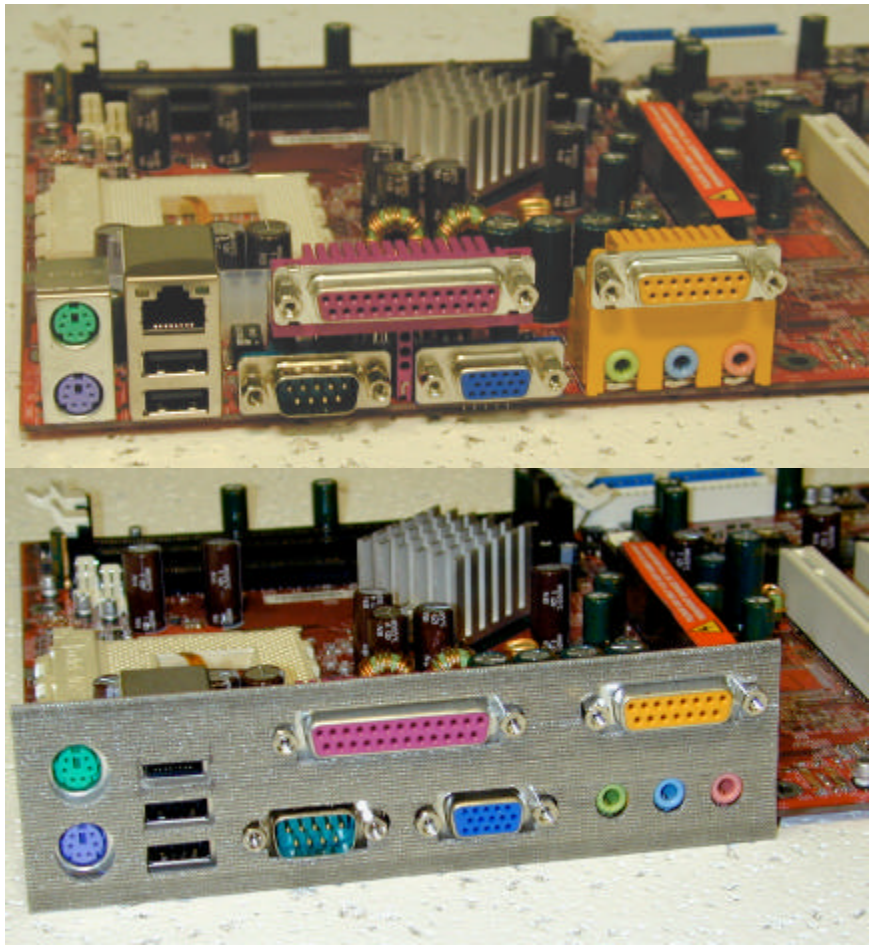
- Filter all signals exiting the system enclosure. Recommend R/C for shielded I/O cables and CMC for unshielded I/O cables. I/O cables must be kept free of EMI noise because cables act as efficient transmitting antennas!
- Dedicate system I/O signal buffer and filter arrays for I/O signals only. Sharing can couple high frequency noise to I/O signals.

I/O Connector Grounding…

- To minimize di/dt noise on I/O cables,
 Either:
 - Isolate the I/O connector post (shield) from mother-board ground through a no-pop 0 ohm resistor; or
 - Moat the ground plane around the I/O connectors. Get expert advice whenever segmenting the ground plane. If done improperly, EMC problems may result.
- I/O cable shields should be bonded to the chassis through low a impedance connection.

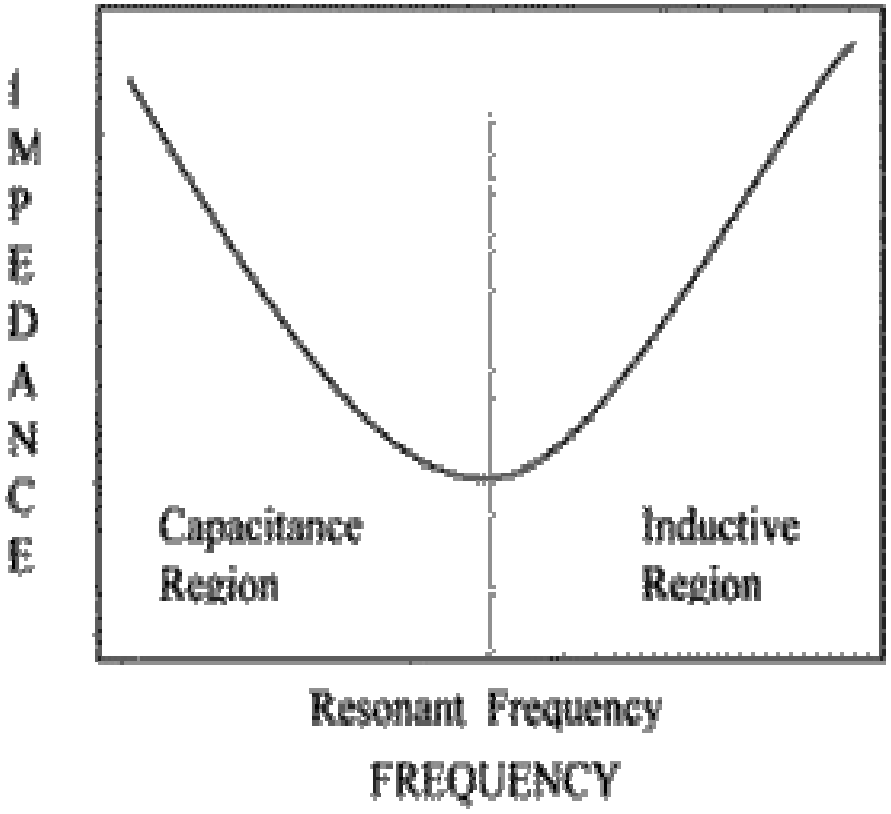
Motherboard I/O Connector EMI Gaskets…

- Provides 360 degree connector bond to chassis.
- Reliable contact made over board placement tolerance.
- Latest gaskets are conductive through the material providing lower impedance.



High Frequency Capacitor considerations…

- Above resonance, a capacitor acts as an inductor.
- Smaller capacitor values have higher self resonance.
- Use low ESL/ESR ceramic 603 / 805.



Decoupling, Filtering, and Stitching Capacitors…

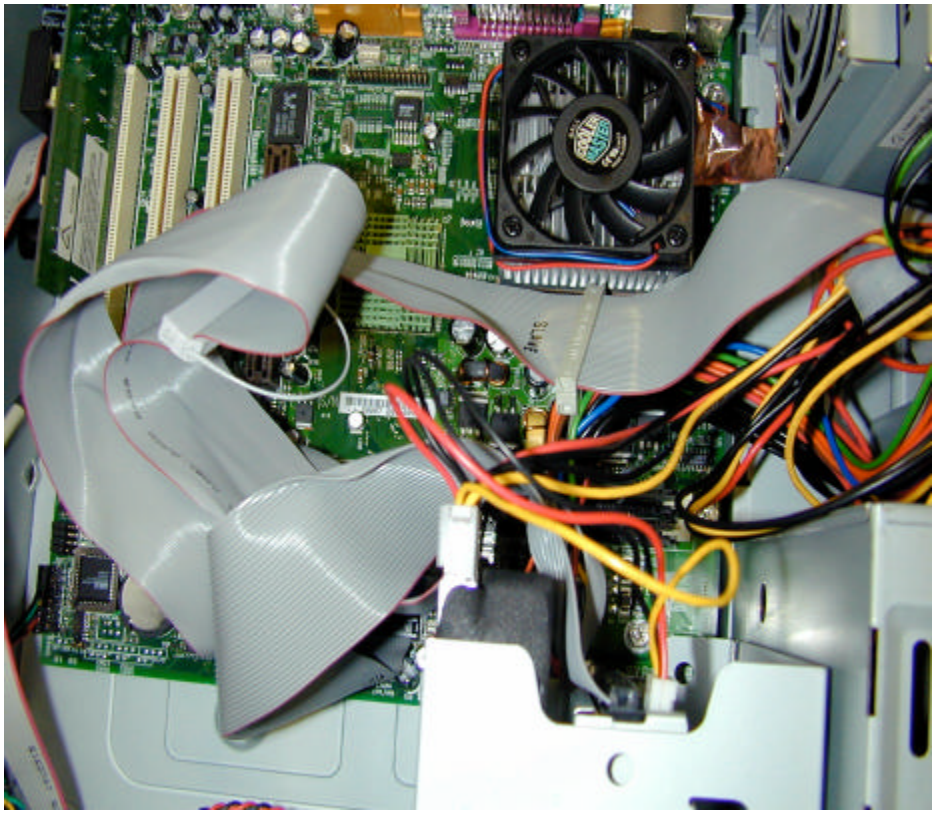
- Closely follow all chip vendor voltage filtering and decoupling guidelines (especially on PLL and Analog voltages).
- Include sufficient high frequency voltage plane bypass capacitors to cover each module voltage pin. (Ex. 0603-X7R-1nF)
- Include sufficient high frequency voltage plane stitching capacitors to be placed within 0.5” of a high speed signal crossing a reference plane break. (Ex. 0603-X7R-1nF)

Component and Connector placement considerations…

- Place noisy clock, CPU and Vreg circuits 1.5” or further away from I/O connectors.
- Place clock series terminating resistors within 1” of source output.
- Place internal cable connectors such that cable routing is away from noisy clock, CPU and Vreg circuits.

Poor Cable Management…

- DC power cables and ribbon cables are too close to EMI noise sources such as CPU, Memory, and Vreg.
- When cables are not secure, there is no repeatability in EMI measurements.



Isolate EMI Source and Victim.

- Route clocks away from I/O signals and board edge. Never route clocks over a reference plane break.
- Place I/O signal filter components as close as possible to their connectors. Then place the I/O driver/receiver modules close to filter components. Route I/O signals directly and in a group. Leave an open isolation channel between I/O & non-I/O signals.

Create a low Impedance Ground…

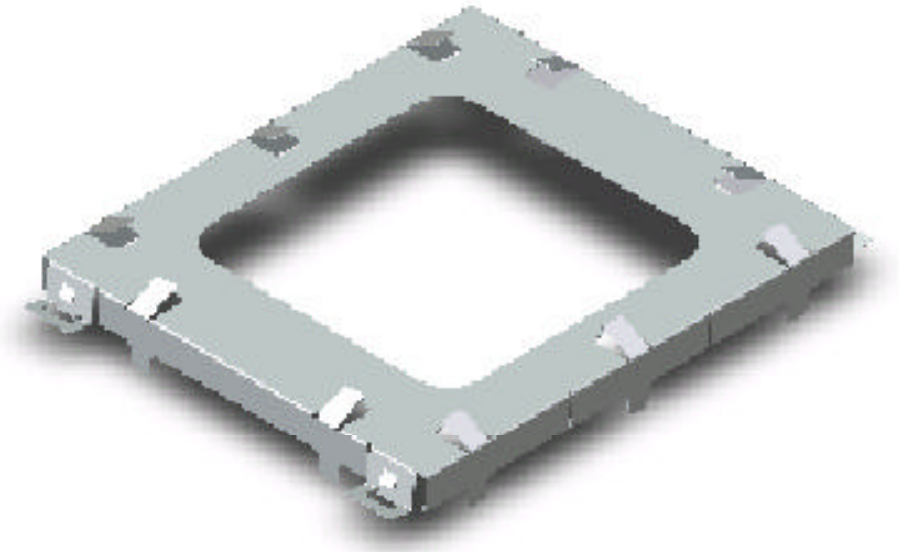
- Make sure all component voltage and ground connections are low impedance. In practice this means using short wide connecting traces to the motherboard voltage or ground planes.
- Multi-via connect the chassis screw mounting pad to the motherboard ground plane (minimum 4 vias per pad).

Processor level EMC Design…

- Integrated CPU Faraday cage grounding.
- CPU package level high frequency voltage decoupling.
- CPU “On-die” voltage decoupling.
- Differential clocking.
- Support for Spread Spectrum Clocking.

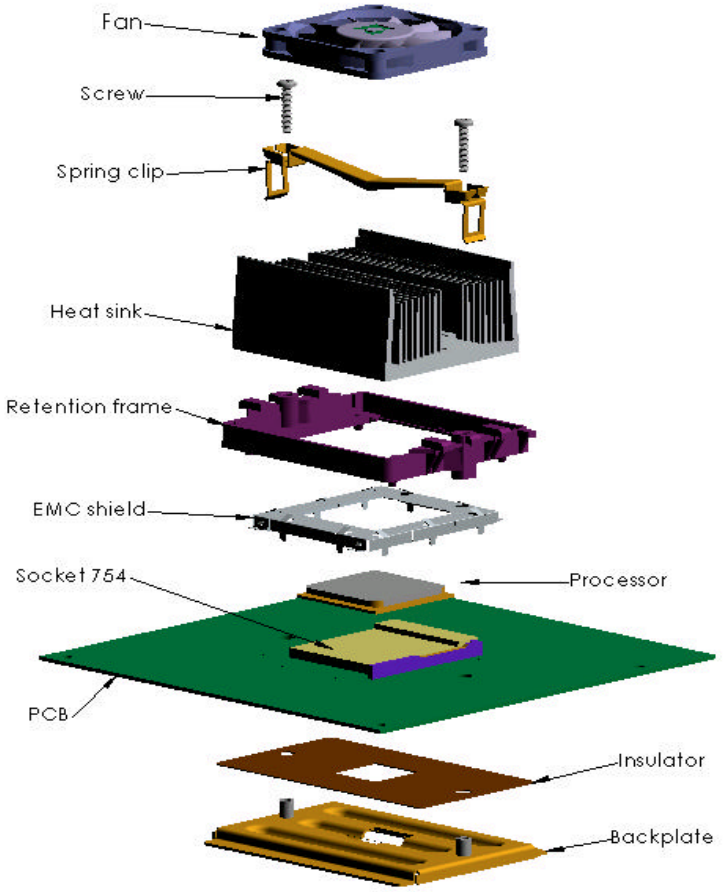
CPU EMC Cage design…

- CPU EMI containment between heat sink and motherboard ground.
- EMC cage bonds heat sink to motherboard ground potential.
- Final design less than ideal Faraday cage. Many, many design constraints.

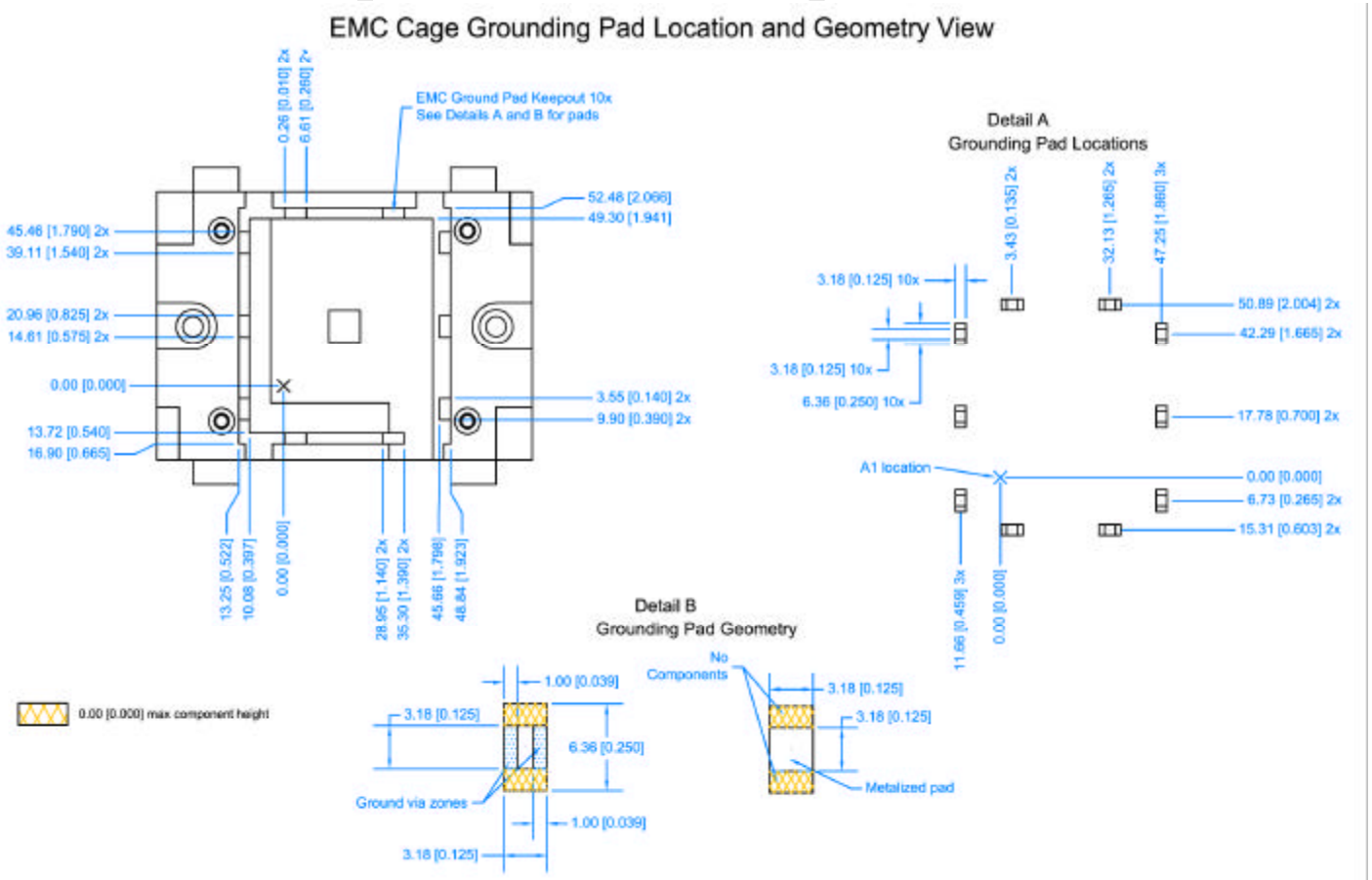


Integrated CPU EMC cage…

- EMC cage is captured between the CPU heat sink and motherboard.
- Installed on “as needed” basis, depending on the system’s shielding effectiveness.
- The motherboard CPU footprint has multiple EMC cage ground pads.



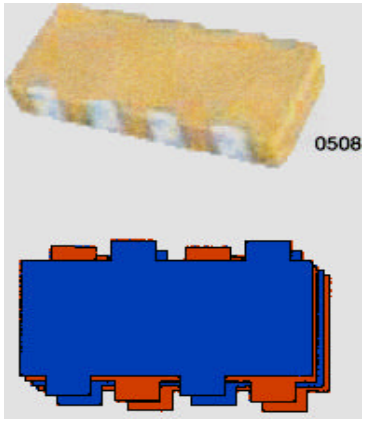
Motherboard CPU EMC Cage ground pad footprint…

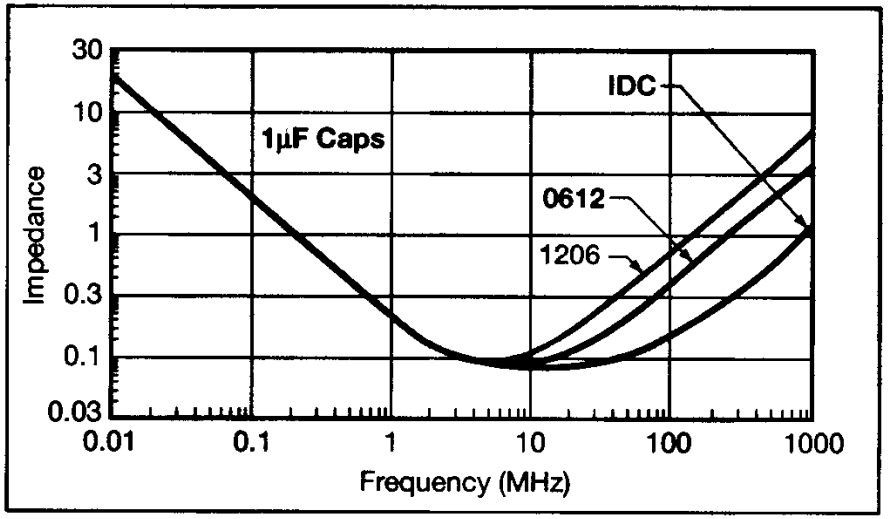


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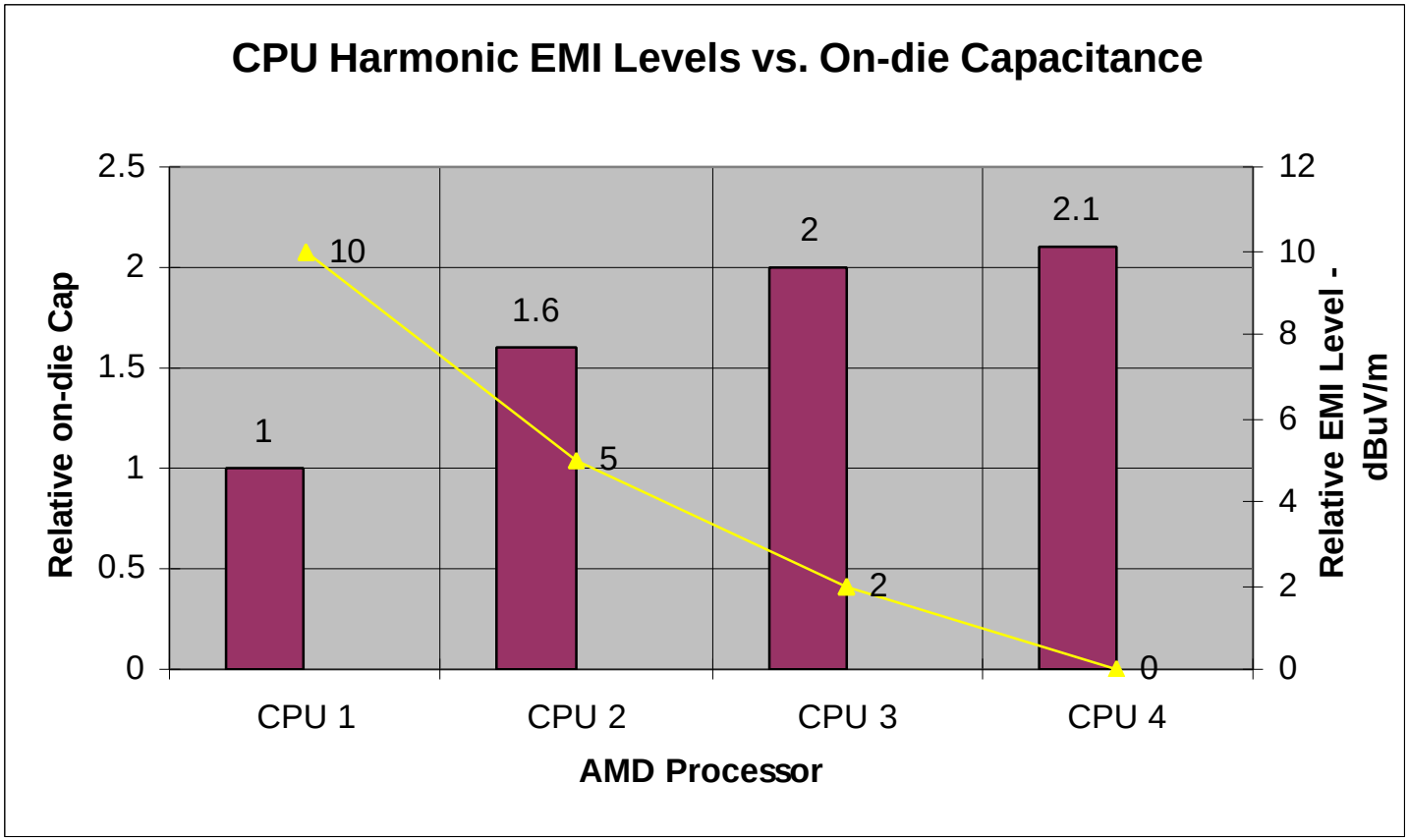
CPU Package level decoupling Capacitors…

- The IDC capacitor construction provides lower inductance. 120 pH (for 0612) and 95 pH (for 0508)
- Opposing current flow in adjacent terminals causes fields to cancel, reducing the equivalent series inductance.



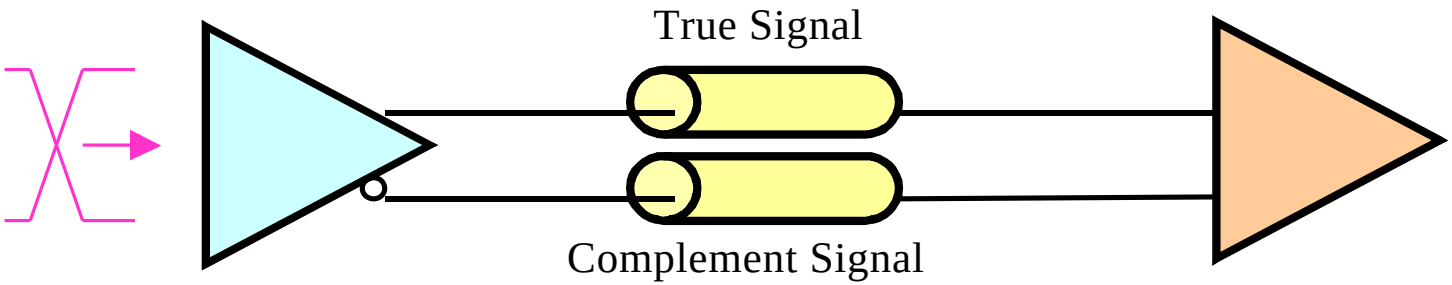


Effect on CPU EMI levels due to On-die Capacitance…



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Differential Signaling….



- Reduced simultaneous switching noise and ground bounce.
- Controlled and reduced loop area reduces EMI.
- Field cancellation from opposing currents.
- Not “as” dependent on a reference plane.

Related AMD Documentation Available under NDA:

- ✓ Hammer Clock Generator Specification (order# 24707)
- ✓ Hammer Processor Family Desktop VRM Design Guide (order# 24901)
- ✓ SledgeHammer Processor Motherboard Design Guide (order# 25180)
- ✓ ClawHammer Processor Motherboard Design Guide (order# 24665)

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